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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,834	07/14/2003	Koji Wakayama	H-1100	5217
<div>7590 08/14/2007 Mattingly, Stanger & Malur, P.C. Suite 370 1800 Diagonal Road Alexandria, VA 22314</div>			<div>EXAMINER WONG, XAVIER S</div>	
			<div>ART UNIT 2616</div>	<div>PAPER NUMBER</div>
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/617,834

Applicant(s)

WAKAYAMA ET AL.

Examiner

Xavier Wong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 21st May 2007.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 2 and 3 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 & 4-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) ✓
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

- ◆ Applicant's Amendment filed 21st May 2007 is acknowledged
- ◆ Claims 1 and 5 – 16 have been amended; claims 2 – 3 are cancelled
- ◆ Claims 1 and 4 – 16 are still pending in the present application
- ◆ This action is made FINAL

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims **1**, **10**, **12** and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Fukumoto et al.** (U.S Pub 2003/0012139) in view of **Gilbert et al.** (U.S Patent 6,771,595 B1).

Consider claims **1**, **12** and **16**, **Fukumoto et al** disclose an apparatus and method of transmitting packets comprising: a plurality of line cards with interfaces for transmitting and receiving packets (paragraphs 0037; fig. 1 items 1-1~N, Lines#0~N); switches connected to the line cards (paragraph 0037; fig. 1 item 2); a processor connected to the switches (paragraph 0038; fig. 1 item 3). **Fukumoto et al** disclose line cards have the capability to monitor / count the amount of packets during communication and determine an outgoing path in reference to (analyzing) a header imparted to IP packets (paragraphs 0037-38; *abstract*; claim 1). Though **Fukumoto et al** did not mention the statistic information collecting function in the processor. It would have been obvious to incorporate the teachings of a statistic information collection function (of the line card) into the processor to perform the same function.

However, **Fukumoto et al** did not explicitly disclose the processor selects transmission interfaces based on the packets amount prediction. **Gilbert et al** disclose a statistic monitoring agent and expert system that predicts future traffic patterns (such as number of packets) and select an (NIC) interface based on the predictions (col. 3 ln. 38-45; col. 4 ln. 5-12). It would have been obvious to incorporate the teachings of a processor that selects transmission interfaces based on the packets amount prediction as taught by **Gilbert et al**, in the apparatus and method of **Fukumoto et al**, in order to dynamically reallocating network resources amongst multiple network interfaces.

Consider claim 10, and as applied to claim 1 above, **Fukumoto et al.**, as modified by **Gilbert et al.**, clearly show and disclose a plurality of line cards *each* comprising a switch interface section and counter section and a function to monitor the amount of received packets during communication and determine an outgoing path with reference to information header (shows a relationship of header information corresponding to amount of received packets) through memory#1 and memory#0 (table) of received IP packets (paragraphs 0037-38 & 0040-42; *abstract*; claim 1); wherein memory#1 and #0 show each line cards and therefore; showing a relationship of a correspondence between header information and an output line card [through the destination port] (paragraphs 0040-41 & 0053; fig. 1 port \leftrightarrow line card links; fig. 9). Though **Fukumoto et al** did not explicitly disclose that a processor acts as a statistic information collecting function along with a table (instead **Fukumoto et al** disclose the statistic information collecting functions in the line card), it would have been obvious to one of ordinary skill in the art to incorporate the teachings of a processor for performing similar functions. It

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also would have been obvious to incorporate the teachings of an apparatus that contains a table (memory) that stores information from a received packet and its destination as taught by **Fukumoto et al**, as modified by **Gilbert et al**, in order to match packet sources and destinations.

Claims **4** and **11** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gilbert et al. (U.S Patent 6,771,595 B1) Fukumoto et al.** in view of (**U.S Pub 2003/0012139**) as applied to claim **1** above, and in further view of **Manning (U.S Patent 6,473,400)**.

Consider claim **4**, and as applied to claim **1** above, **Fukumoto et al.**, as modified by **Gilbert et al.**, clearly show and disclose the claimed invention except that the apparatus comprise a bus that directly connects the interfaces and statistic information collecting processor. In the same field of endeavor, **Manning** disclose a packet processing device 2, which utilizes data from RMON table 7 (a statistic collector) through analyzer 6, are directly connected to a plurality of ports/interfaces 1 through a bus (column 3 lines 26-45; fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of an apparatus that comprises a bus for directly connecting interfaces and a statistic information collecting processor as taught by **Manning**, in the apparatus of **Fukumoto et al.**, as modified by **Gilbert et al.**, in order to access packet information more rapidly.

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Consider claim **11**, and as applied to claim **10** above, **Fukumoto et al.**, as modified by **Gilbert et al.**, clearly show and disclose the claimed invention except that the table data is renewable. In the same field of endeavor, **Manning** clearly discloses that the RMON table can be updated if further data samples are acquired (column 5 lines 40-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of an apparatus that the table is renewable as taught by **Manning**, in the apparatus of **Fukumoto et al.**, as modified by **Gilbert et al.**, in order to maintain the newest packet information in record.

Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Fukumoto et al. (U.S. Pub 2003/0012139)** in view of **Gilbert et al. (U.S. Patent 6,771,595 B1)**, as applied to claim **1** above, and in further view of **Born (U.S. Patent 6,631,484)**.

Consider claim **5**, and as applied to claim **1** above, **Fukumoto et al.**, as modified by **Gilbert et al.**, clearly show and disclose the claimed invention except wherein the interfaces have means for storing, in a frame, at least a portion of a header imparted to at least one or more packets. In the same field of endeavor, **Born** discloses an interface apparatus that comprises packet storage/memory in a FIFO stack (column 7 lines 9-20; claims 29 & 31) and storing header in the FIFO stack (column 9 lines 38-49; claim 41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of an apparatus that has the capability to store header information as taught by **Born**, in the apparatus of **Fukumoto**

et al. as modified by **Gilbert et al.**, in order to facilitate the extraction of packet information.

Claims **6**, **7** and **13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Fukumoto et al. (U.S. Pub 2003/0012139)** in view of **Gilbert et al. (U.S. Patent 6,771,595 B1)** and in further view of **Born (U.S. Patent 6,631,484)**, as applied to claim **5** and **12** above, and in further view of **Agarwal et al. (U.S. Patent 6,819,165 B1)**.

Consider claim **6**, and as applied to claim **5** above, **Fukumoto et al.** in view of **Gilbert et al.** and in further view of **Born** clearly show and disclose the claimed invention above except headers that are to be multiplexed into a frame have equal size. In the same field of endeavor, **Agarwal et al.** disclose headers, all one byte (same size), are applied to data in packets; while packets greater than a minimum size are to be remained temporarily to be divided / segmented into SAR2 headers and multiplexed / gathered back into a packet / frame and be forwarded to a modem at a terminal (col. 11 ln. 61-67; col. 12 ln. 1-16; fig. 11A). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of an apparatus that multiplexes / gathers headers (along with their respective packets) to a terminal as taught by **Agarwal et al** in the apparatus of **Fukumoto et al**, in order to identify packet destination.

Consider claim **7**, and as applied to claim **5** above, **Fukumoto et al.** in view of **Gilbert et al.** and in further view of **Born** clearly show and disclose the claimed

invention above except that means for multiplexing determines length of a header portion to be extracted from a plurality of packets in response to information indicating classification of the packets and that the packets are to be multiplexed into one frame. In the same field of endeavor, **Agarwal et al.** disclose an apparatus that is able to distinguish header sizes, which are of 1 byte and 3 bytes respectively for SAR1 and SAR2 classification packets; and the extraction of the headers (column 11 lines 61-67 & column 12 lines 1-17; fig. 11A). 3 byte cells are [stored] for division / segmentation into SAR2 headers before the headers are then being multiplexed and stored into a packet / frame and be sent to a terminal (column 12 lines 25-29). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of an apparatus that comprises means for multiplexing determines length of a header portion to be extracted from a plurality of packets in response to information indicating classification of the packets and that the packets are to be multiplexed into one frame as taught by **Agarwal et al.**, in the apparatus of **Fukumoto et al.**, as modified by **Gilbert et al.**, and **Born**, in order to identify each of the packets.

Consider claim 13, and as applied to claim 12 above, **Fukumoto et al** in view of **Gilbert et al**, and in further view of **Born**, clearly show and disclose the claimed invention above except the multiplexing of header information into a frame. In the same field of endeavor, **Agarwal et al.** disclose packets that are greater than a minimum size are to be remained temporarily to be divided / segmented into SAR2 headers and multiplexed/gathered back into a packet / frame (col. 11 ln. 61-67; col. 12 ln. 1-16; fig.

11A). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of a method that multiplexes/gathers headers (along with their respective packets) to a terminal as taught by **Agarwal et al**, in the apparatus of **Fukumoto et al**, as modified by **Gilbert et al** and **Born**, in order to identify the destination of the packets.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Gilbert et al. (U.S Patent 6,771,595 B1)** in view of **Fukumoto et al. (U.S Pub 2003/0012139)**, as applied to claim 1 above, and in further view of **Chiussi et al. (U.S Patent 7,027,457)**.

Consider claim 8, and as applied to claim 1 above, **Gilbert et al.**, as modified by **Fukumoto et al.**, clearly show and disclose the claimed invention except the apparatus comprises a plurality of statistic information collecting processors. In the same field of endeavor, **Chiussi et al.** disclose a plurality of packet counters (230-CNT, 240-CNT, 330-CNT, etc.) monitors the number of data packets in a traffic flow (column 9 lines 26-56 & column 14 lines 41-56; fig. 2, 6 & 8), which is essentially the function of the claimed statistic information collecting processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of an apparatus that comprises a plurality of processors that collect packet statistical data as taught by **Chiussi et al.**, in the apparatus of **Gilbert et al.** as modified by **Fukumoto et al.**, in order to identify bottlenecks in a network.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Fukumoto et al. (U.S. Pub 2003/0012139)** in view of **Gilbert et al. (U.S. Patent 6,771,595 B1)**, as applied to claim 1 above, and in further view of **Muller et al. (U.S. Patent 6,016,310)**.

Consider claim 9, and applied to claim 1 above, **Fukumoto et al.**, as modified by **Gilbert et al.**, clearly show and disclose the claimed invention except the extension function processor is connected to a load balancing processor and that the extension function processor performs at a higher layer than the layer on which a packet is received. In the same field of endeavor, **Muller et al.** disclose a network device that comprises a Multi-Layer Distributed Network Element (MLDNE) that is configured to handle message traffic using TCP and IP protocols (layers 4 and 3) over Ethernet LAN standard and MAC data link layers (column 3 lines 43-53) while messages/packets are received at a network interface at physical layer 1 input ports (column 5 lines 3-22). The network device also performs load balancing on certain packets (column 11 lines 11-58; claim 23 & 27), therefore, justifying that a load balancing device has direct connection with the MLDNE. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of an extension function processor (MLDNE embodied in network device) is connected to a load balancing functionality (also embodied in network device) and that the extension function processor performs at a higher layer than the layer on which a packet is received as taught by **Muller et al.**, in the method of **Fukumoto et al.**, as modified by

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Gilbert et al., in order to distinguish different types of packets being received and transmitted.

Claims **14** and **15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Fukumoto et al.** (U.S. Pub 2003/0012139) in view of **Gilbert et al.** (U.S. Patent 6,771,595 B1) and in further view of **Agarwal et al.** (U.S. Patent 6,819,658), as applied to claim **13** above, and in further view of **Kojima** (JP 2001-160832).

Consider claim **14**, and as applied to claim **13** above **Fukumoto et al.**, as modified by **Gilbert et al.**, and in further view of **Agarwal et al.**, clearly show and disclose the claimed invention except wherein extracting only a portion of the header from received packet. In the same field of endeavor, **Kojima** discloses the extraction of only the signal component (a portion of the header) of each frame in serial data (*Abstract*). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of a method to extract only a portion of the header, as taught by **Kojima**, in the apparatus of **Fukumoto et al.** as modified by **Gilbert et al.** and **Agarwal et al.**, for the purpose of signal alignment.

Consider claim **15**, and as applied to claim **13** above, **Fukumoto et al.**, as modified by **Gilbert et al.**, and in further view of **Agarwal et al.**, and in further view of **Kojima** clearly show and disclose the claimed invention except a method to indicate classification of packet set to a header to be imparted to each of the packets. **Agarwal et al.** also disclose a method to distinguish header sizes, which are of 1 byte and 3 bytes respectively for SAR1 and SAR2 classification packets and the extraction of the

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headers (column 11 lines 61-67 & column 12 lines 1-17; fig. 11A). The headers are then being sent (multiplexed) into a single terminal (column 12 lines 25-29). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of a method that further comprise a step of extracting a header of said received packet only by a size corresponding to information indicating classification of said packet set to a header to be imparted to each of said packets as taught by **Agarwal et al.**, in the method of **Fukumoto et al**, as modified by **Gilbert et al**, and **Kojima**, in order to identify packets with their corresponding headers correctly.

Response to Arguments

Applicant's arguments filed on 21st May 2007 with respect to claims **1, 4 – 7, 10 – 13** and **16** have been considered but are not persuasive.

Consider claims **1, 10, 12** and **16**, the amended / added "a plurality of line cards" is a missing element from the original (pre-amended) claims; the "plurality of line cards" is disclosed by **Fukumoto et al** in figure 1.

Further consider claims **1, 12** and **16**, **Fukumoto et al**, as modified by **Gilbert et al**, meet the claimed limitations as amended. **Fukumoto et al** show a plurality of line cards with interfaces in figure 1 and figure 2 items 11 & 18; wherein the statistic information collecting processor is interpreted as being obvious to be implemented into processor 3 in figure 1 instead of being in the line card with the processor's functions

clearly emphasized. Please refer to the examiner's revised claim 1 (12 & 16) rejection that explains the concerned details.

Consider claim 4, the applicants basically argue that claim 4 is patentable due to its dependency on rejected claim 1 over **Fukumoto et al** and **Gilbert et al**. The functions performed in the line card of **Fukumoto et al** are interpreted as obvious to be implemented into processor 3 as mentioned above.

Consider claims 10 and 11, **Manning** is made a combination with **Fukumoto et al** and **Gilbert et al** to *explicitly* signify a "table" for source and destination address storage and updating / renewing table on the original (pre-amended) version of said claims; while **Fukumoto et al** mention the remaining limitations such as line cards, header information of packets and the statistics table of claims 10 and 11. Please refer to the examiner's claims 10 and 11 rejections, which explain the concerned details.

Consider claim 5, **Born** is made a combination of **Fukumoto et al** and **Gilbert et al** to explicitly signify storage of a frame/packet on the original (pre-amended) version of said claim. **Fukumoto et al** disclose the remaining limitations such as plural headers imparted to a plurality of packets and interfaces that transmit and receive frames/packets as well as transmitting the frames/packets to the "statistic information collecting processor / line card." Please refer to the examiner's claim 5 rejection, which explains the concerned details.

Consider claims 6, 7 and 13, **Agarwal et al** disclose the process of multiplexing plural headers into a frame / packet. **Agarwal et al** disclose incoming packets that are greater than a minimum size are to be remained temporarily to be divided / segmented

into SAR2 headers and multiplexed / gathered back into a frame / packet as explained in column 11 lines 61-67 and column 12 lines 1-16 and further in figure 11A. Please refer to the examiner's claims 6, 7 and 13 rejections, which address the concerned details.

Consider claims 8, 14 and 15, the applicants basically argue that claims 8, 14 and 15 are patentable due to their dependencies on **Fukumoto et al**, **Gilbert et al**, **Agarwal et al** and **Born et al** which the applicants state the mentioned prior arts are deficient. The examiner hereby confirms all rejections concerning the mentioned prior arts have been addresses above.

Therefore, in view of the above reasons and having addressed the Applicants' arguments, the rejection is respectfully maintained and made **Final** by the examiner.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. This Action Is Made **FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

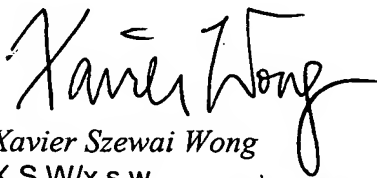
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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is (571) 270-1780. The examiner can normally be reached on Monday through Friday 8 am - 5 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.


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8/7/07


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